Waveform Characterization and Modeling of Dynamic Charge Behavior of InGaP-GaAs HBTs

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***Abstract* — This study presents a novel time-domain characterization method for the first time, to reveal dynamic charge behavior of HBTs. The charge model plays an important role for power InGaP-GaAs HBT amplifiers designed with self-biasing. It is shown that charge-storage and extraction from the base of the HBT at a high-power drive can not be described by conventional quasi-static model. A new collector-base charge model is proposed to account for the time-response of the devices.**

I. INTRODUCTION

Power amplifiers for advanced wireless handsets are required to have single polarity bias, high efficiency and low distortion. HBTs have proven to be a competitive candidate. To predict the power performance, dc and bias-dependent S-parameters, it requires an accurate HBT model, including charge model.

During the last few years, a number of HBT models have been proposed with emphasis on self-heating effects [1][[2][3][4][5]. Some of them also take into account the non-quasi-static charge [4][5]. Trans-capacitance of base-collector has been shown to have higher-order effects on HBT performance, namely linearity and distortion. Otherwise, there is no clear-cut evidence of its effects on transient response and power performance. A GP HBT model combined with self-heating modeling is sufficient to fit dc as well as small-signal response at various forward operation biases. However, it is found that this classic model fails to generate accurate large-signal time response at a high power drive, especially when there is a self-biasing resistor in the base bias circuit. Self-biasing is widely utilized in power amplifiers to enhance stability, help to eliminate thermal corruption.

Time-domain characterization has been recognized as a valuable tool for modeling of transistors and diodes [6][8]. The time response can be used to reveal non-quasi-static effects of devices, for instance, in a step-recovery diode. In this paper we present a method of waveform characterization as a supplemental extraction approach to the conventional bias-dependent S-parameter approach, to de-embed the non-quasi-charge behavior.

II. DANAMICAL CHARGING REVEALED BY WAVEFORMS

Waveform measurement technique has been presented elsewhere (4). The system was vector-calibrated with 50 ohm terminated. The fundamental was 0.9 GHz and 8 harmonics were measured. The transistors used in this work were GaInP/GaAs HBTs of four unit cells, each of 240 um^2 emitter area with two emitter fingers of 3um by 40um and a ballast resistor of 40 ohm on the base. The input power is from 11 to 13 dBm and quiescent collector current was 70 mA at Vc=3.2 V. The driving power is sufficient to swing the collector voltage to saturation region where both junction are partially conductive.

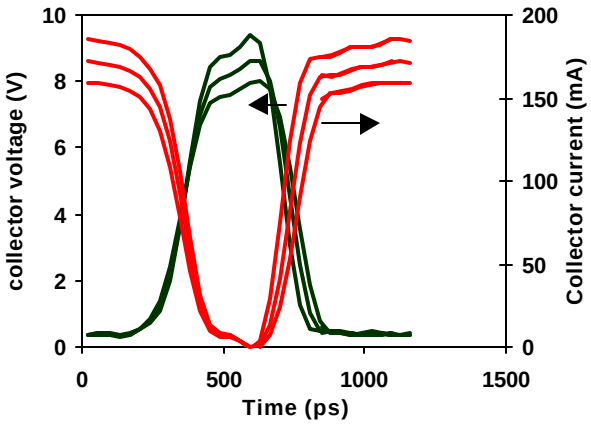

Figure 1. Collector voltage and collector current waveform of a 960 um^2 HBT. Vco=3.2V, Vbeo=1.28V and Pin=11,12 and 13 dBm.

Fig.1 shows the collector voltage and collector current waveforms. Given that the parasitic resistances and inductances are de-embedded as described in section III. The intrinsic base-emitter voltage Vbei and intrinsic base-collector voltage Vbci can be calculated as shown in Figure 2, in that the base current is also plotted. It is shown that the Vbei is clamped around at Vbei=1.3 V where the base-emitter junction is at forward, as expected. The Vbci , however, is clamped at around or less than 1.0V,

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far below the collector-base built-in voltage, 1.23 V measured from DC. The base current, as shown in fig. 2, swings from positive to negative during the time period where the Vbci or Vbei is kept clamped. The time response of current is a resemblance of that of microwave step-recovery diode under RF drive. When the RF current swings to negative, the junction is kept at forward until all the charges stored at junction is extracted out. Obviously, the quasi-charge model is not applicable here. A good description of non-quasi-static charging effects is assuming an infinite or a very high capacitance at clamped voltage. The infinite capacitance model is valid for an ideal case of non-charge consumption in the base, neither by recombination nor by extraction of opposite junction field.

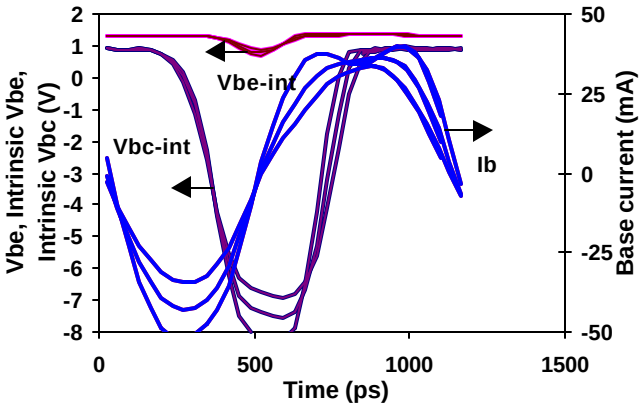


Figure 2. Intrinsic base-emitter voltage and intrinsic base-collector current waveforms of a 960 um^2 HBT. Vco=3.2V, Vbeo=1.28V and Pin=11,12 and 13 dBm

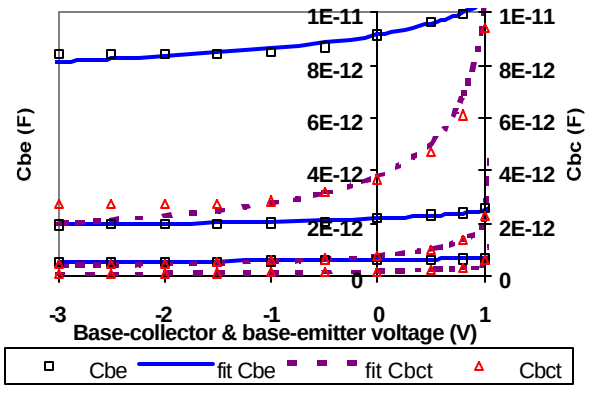


Figure 3. Measured (symbol) and fitted (line) base-collector and base-emitter capacitance vs. base voltage for 240, 960 and 3840 um^2 devices, respectively from top down.

A very high capacitance at Vbc of about 1V is, however, contradictory to the measured values from S-parameters, as shown in figure 3, where no extraordinarily high capacitance at Vbc=1 V can be seen. In order to be consistent with small-signal models at various biases, we assume that the base-collector charge storage at saturation region is also a function of base-emitter voltage. A forward BE-junction creates charge storage at the BC junction due to an enhanced emitter barrier. At Vbci=1 V the field of collector space-charge-region becomes too small to drift the charges to the collector, leaving the base charges waiting for extraction at a reverse base current. Thus the effective turn-on voltage for charging becomes 1 V instead of 1.23V.

III. HBT MODEL EXTRACTION AND MODIFICATION

To extract large-signal model of HBTs, dc, thermal and S-parameter characterization have been utilized. Conventional Gummel-Poon model in conjunction with self-heating circuit is found sufficient to fit Ic-Vc and Vbe-Vc curves. The self-heating effects are modeled by a thermal-subcircuit and two nonlinear feed-back circuits, a shown in fig.4, one used to model the decrease of Vbi of junctions with temperature, the other models the decreases of current gain. The capacitance-voltage dependencies of both junctions are extracted at Vbe<1.2 V and Vbc<=1.0 V or cut-off conditions, as shown in figure 3. The forward and collector transit time as function of Vcb and Ic is extracted from S-parameters at forward biases. The extraction approach of charge-related parameters and parasitic resistances and inductances are described previously [7].

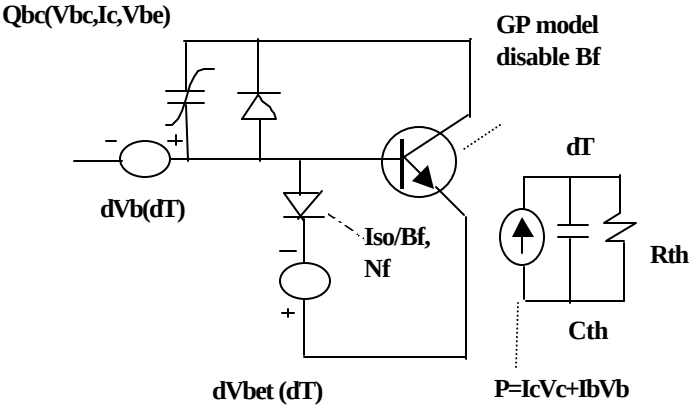


Figure 4. Schematic of intrinsic HBT model consisting of a GP HBT model, thermal circuit, two feedback sources and modified BC charge

It is found that the model generated is adequate to be able to fit the S-parameters at both forward and reverse operation regions. There are some problem to fit S-parameters at saturation region. Inclusion of trans-capacitance associated with current and transit time, as described in (5), was made to help to fit the measured results a at high current region. It turns out, however, that it is difficult to accurately de-embed the junction

capacitance at heavy forward bias because of the shunting by the junction conductance.

To account for the apparent clamping of Vbei at lower voltage, we introduce a modified collector charge term $Q_c(V_{bceff})+I_c\ \tau_c$, where Qc is the original charge model as function of V_{bc}, and $V_{bceff}= V_{bc} + V_{be'}$. The collector capacitance then can be expressed as

$$C_{bc}(V_{bc}, V_{be'})= C_{bco}(I_c)/(1-(V_{bc}+V_{be'})/V_{bi})^m \quad V_{bc}+V_{be'}<f_c\ V_{bi} \qquad (4)$$

$$C_{bc}(V_b, V_{be'})= C_{bco}(I_c)/(1-f_c)^m(1-f_c(1+m)+mV_{bc}/V_{bi}) \quad V_{bc}+V_{be'}<f_c\ V_{bi} \qquad (5)$$

Where

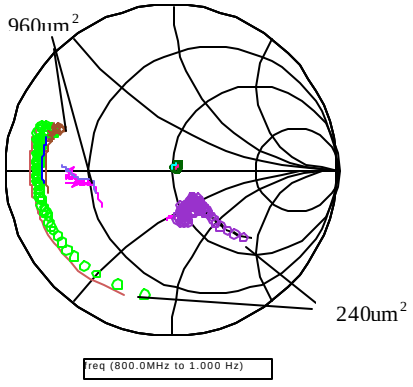
$$V_{be'}= g\,(1+\tanh(f(V_{be}-U))) \qquad (6)$$

and g, f and U are the fitting parameters. U is somewhere below the B-E building voltage. Essentially, a forward base-emitter voltage modifies the B-C build-in voltage by $V_{be'}$ and the modified value becomes zero when V_{be} drops to below U-1/f. Here fc is assumed close to 1, to say 0.98. Therefore, the Cbc becomes very high when Vbc is equal to 1.23V-Vbe'.

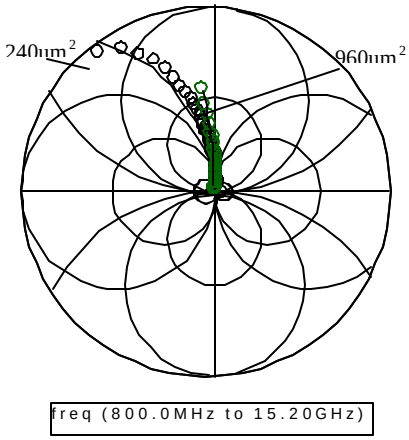
Apparently, the modification does not significantly affect the base-collector capacitance characteristics at reverse active region where the emitter junction is at cutoff. The change of collector charge at forward operation region is a minor factor because the capacitance varies with V_{bc} insignificantly for a negative bias. Thus the modification occurs mostly at saturation region.

IV. Extraction and Modeling Results

In addition to 240 um^2, 960 um^2 and 3840 um^2 are also measured for scalability study. The transistor was ballasted for thermal stability. The thermal resistance Rth is measured and fitted by a formula, Rth= 46639x(Ac)$^{-0.7463}$. Self-heating effect on built-in voltage is modeled by $\delta V=-0.0012*\delta T*\exp(\delta T/To)$ and its effect on current gain is expressed by a nonlinear term $\delta\beta=-0.014*\delta T/(To*nf*Vt)*\exp(\delta T/To)$. The dc and parasitic related parameters for unit cell are:



(a)



(b)

Figure 5. Model (line) vs measured (symbol) for S11,S12,S22 (a) and for S21(b), respectively. Both 240 and 960 um^2 are plotted in the same figure.Vc=3V, Ic=13mA per 240 um^2.

Iso=1.52e-24, Nf=Nr=1.008, Bf=133.0, Ise=1.53e-22, Ne=1.285, Isc=1.2e-14, Nc=1.88, Br=0.4, xcjc=0.63, Re=0.353, Rbi=0.55, Rbx=1.046 and Rc=1.144.

The charge related parameters are:

Cjc=0.205pF, Vjc=1.23, mc=0.55, Cje=0.523pF, Vje=1.4 me=0.08, Tfo=8ps, xtf=0.7, vtf=-5, Itf=0.13A and Tr=50ps.

The parameters associated with charge modification are: g=1.2, U=1.18, and f=4.

It is found that the model is scaleable up to 3840 um^2 in terms of reproducing dc and s-parameters at various biases. The fitting error is within 5% for both Vbe vs Vc and Ic vs Vc curve families. Figure 5a and 5b, shows respectively the comparison of modeled s11, s12, s22, and s21, respectively, for a 240 um^2 unit cell and 960 um^2 devices using a unified scaleable large-signal model. To be scaleable, the scaling rule for extrinsic resistances and inductances are experimentally determined and fitted by nonlinear expressions.

In order to validate the proposed model for large-signal response, the simulated time response of the device at a 50ohm-termination condition is compared to the measured. Figure 6 and 7, respectively, shows the simulated verses measured time response of Vb(t) and Ib(t), and waveforms of intrinsic Vbe(t) and intrinsic Vbc(t). It is shown indeed that the intrinsic Vbc clamped at about 1V and the waveforms compare to the measured very well.

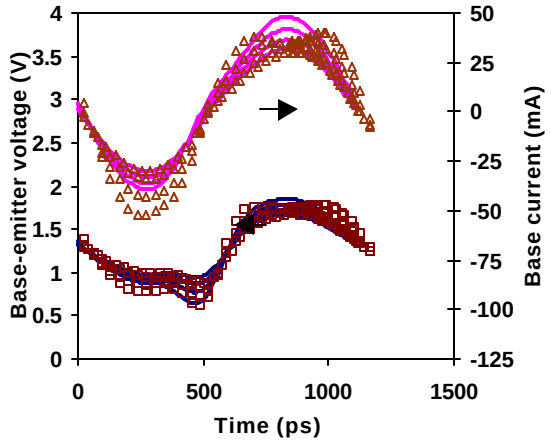


Figure 6. Modeled (line) vs measured (symbol) base voltage and base current waveforms. F=0.9GHz, Vc=3.2V, Vbo=1.28V, Pin=11,12 and 13 dBm.

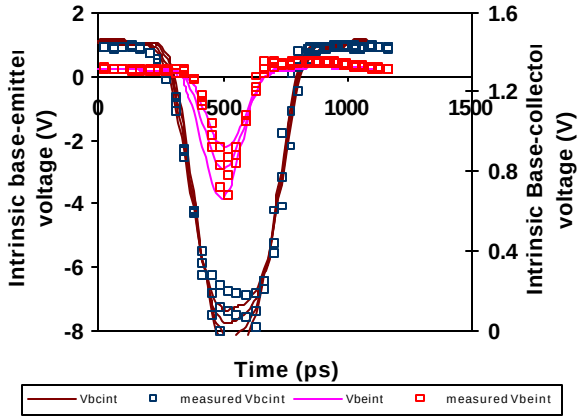


Figure 7. Modeled (line) vs measured (symbol) intrinsic B-E voltage, B-C voltage. F=0.9GHz, Vc=3.2V, Vbo=1.28V, Pin=11,12 and 13 dBm.

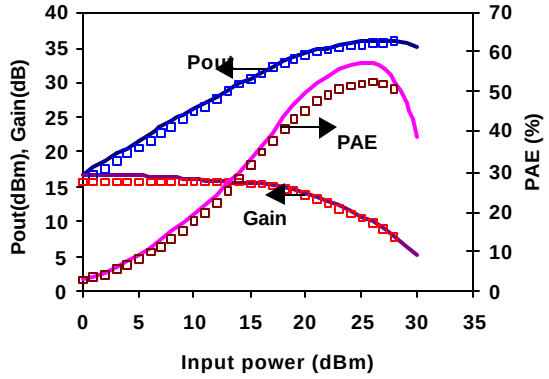


Figure 8. Simulated (line) vs measured (symbol) power performance of last stage of a GSM amplifier, Vc=3.2V, Ico=0.4A.

The model was further verified in simulation of a real GSM power amplifier. The last stage of power amplifier is a 7840 um^2 device with an input capacitance tuning and a self-bias resistance. Figure 8 plots the simulated vs measured output power, power-added efficiency and power gain as functions of input power. The power output is limited by the self-biasing because of the negative move of the base bias voltage. Classic model generates more serious self-biasing than measured and it wrongly predicts 1.2 dBm lower power but 15% higher PAE. Owing to the dynamic charge injection and extraction in the new model, less charge storage is resulted on the external capacitance, leading to higher power output.

V. Conclusion

Time-domain measurements have revealed the dynamic charge or non-quasi charge behavior of InGaP-GaAs HBTs. A new charge model is present to account for the dynamic charging effects. In addition to excellent fitting to the dc, S-parameters, the model successfully predicts the time response and power performance for power amplifier, which, therefore, validated the model. The model is accurate, temperature-dependent and scaleable and it can be used for wireless power amplifiers where self-biasing and large-sized devices are employed.

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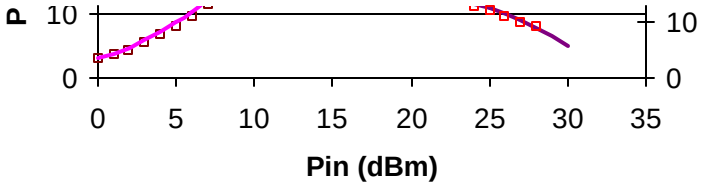

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